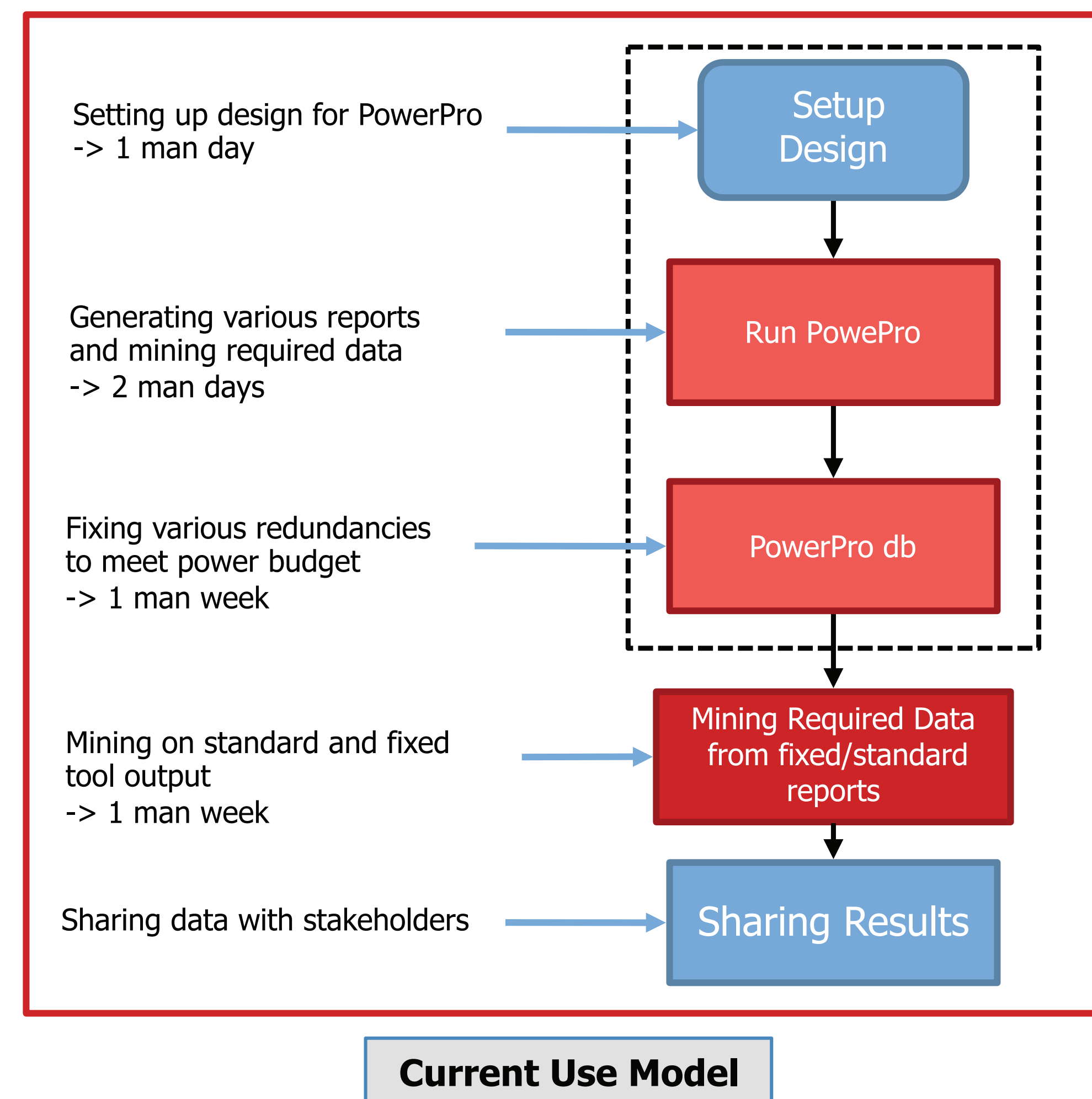


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## Motivation: Why is a Metric Driven Approach Needed?

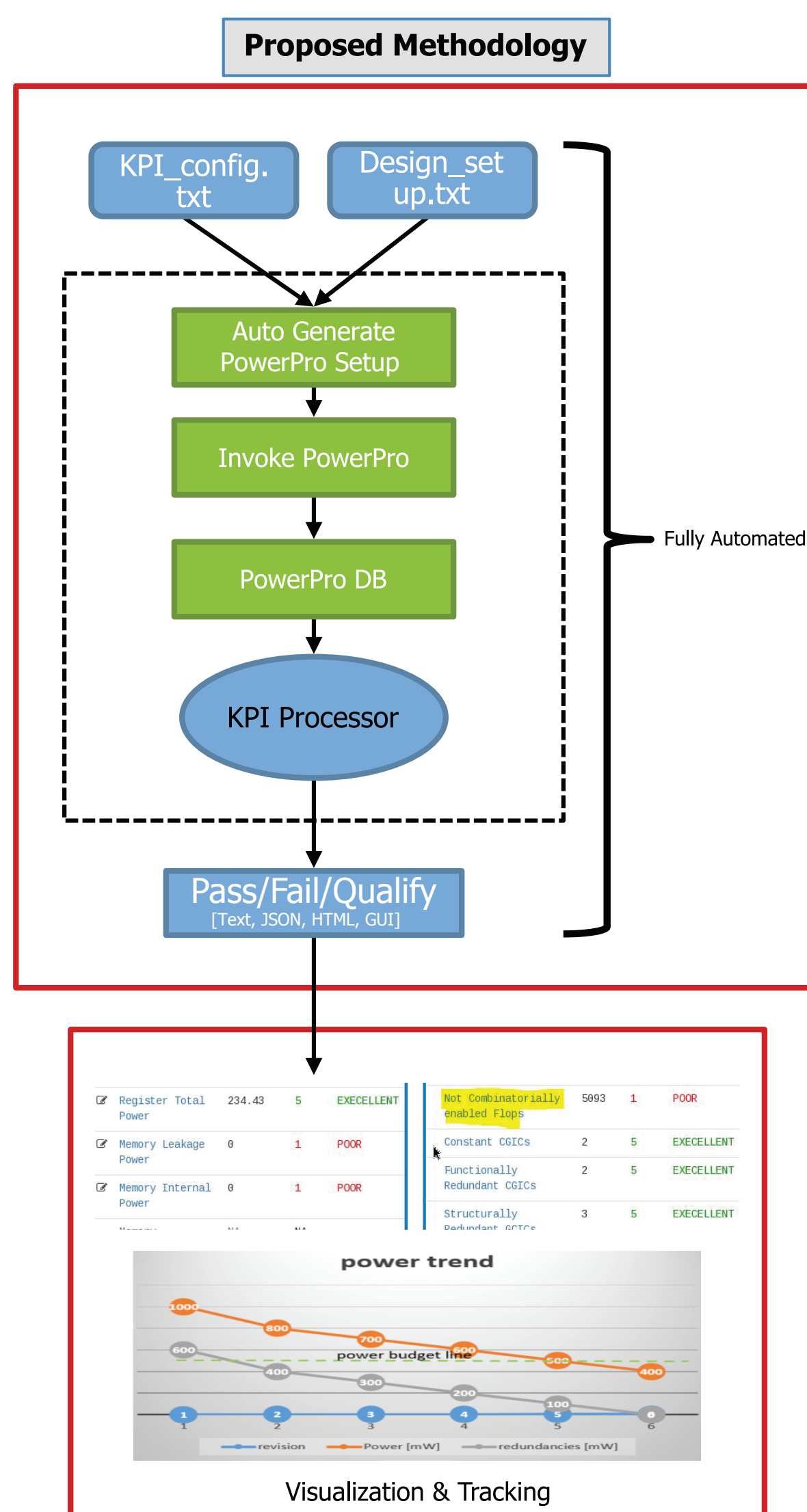
- Power tools often used as point tools and require expert users to generate meaningful data.
- Needed a mechanism to define confidential/proprietary recipe for power tracking which is unknown to even vendor.
- Huge information gap between user and management regarding power scenario of the block/chip.
- Needed a methodology based regression framework for quick and easy insight.
- Needed an automated method to work upfront on predefined objective [KPIs] rather than generating humongous data and thereafter mining it via scripting to qualify/track those objectives.
- Needed an automated flow to quickly qualify the block/chip for power.
- Need an automated way to quickly qualify the usecase [IDLE/AVERAGE/PEAK]
- Metric based check-points on vital power related parameters of the chip.
- Redundancies, toggle, and power estimation trend monitoring via graphs and plots with each revision of the RTL.
- Easy mapping of real issues and single cockpit debugging environment
- Easy integration into existing regression frameworks.
- Easy sharing of data across teams via HTML pages.
- Caters to IP regression suite as well as SoC with multiple runs across the design cycle and for multiple users.



## Proposed Solution: Metric Driven Power Regression

### The Solution:

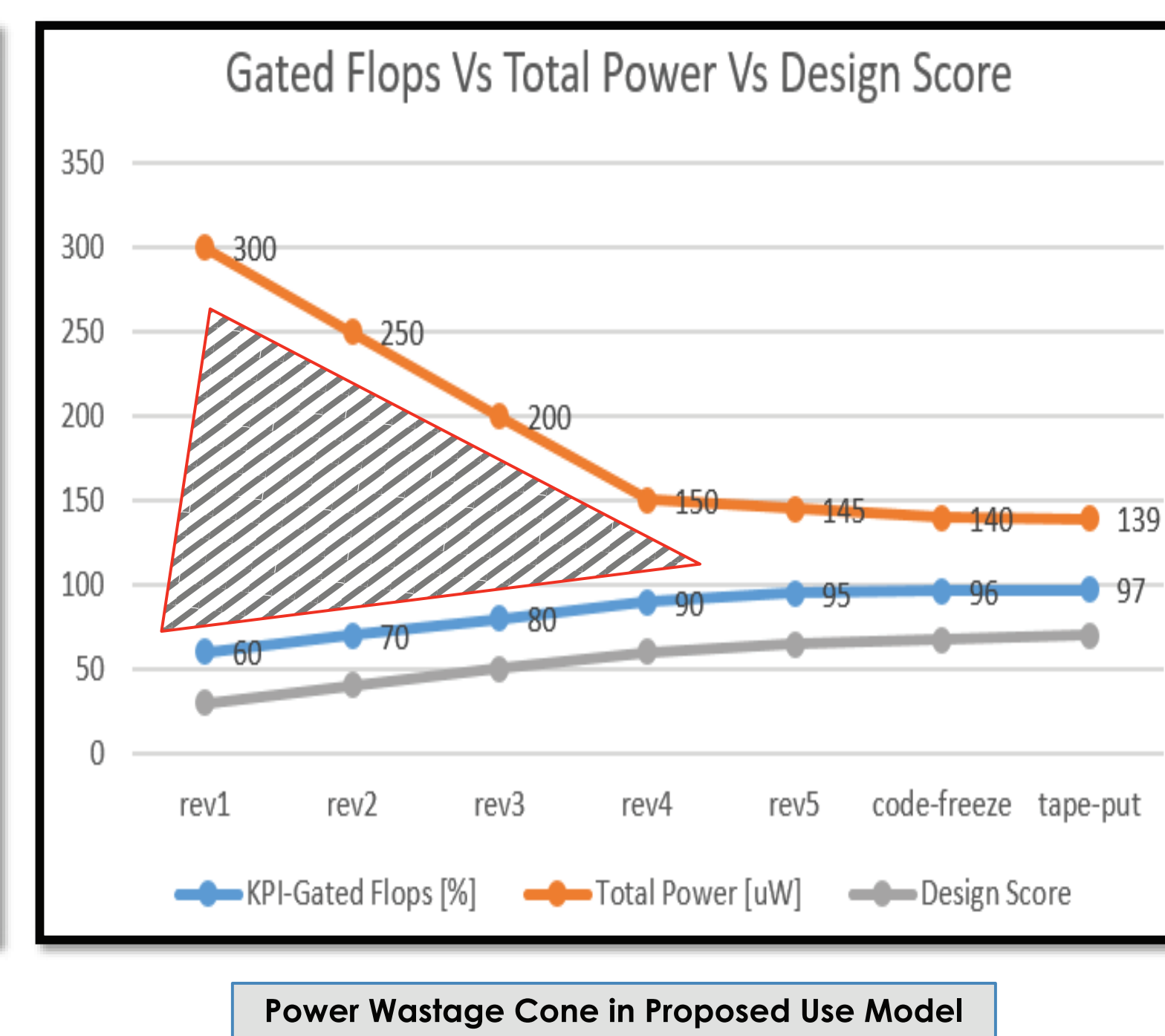
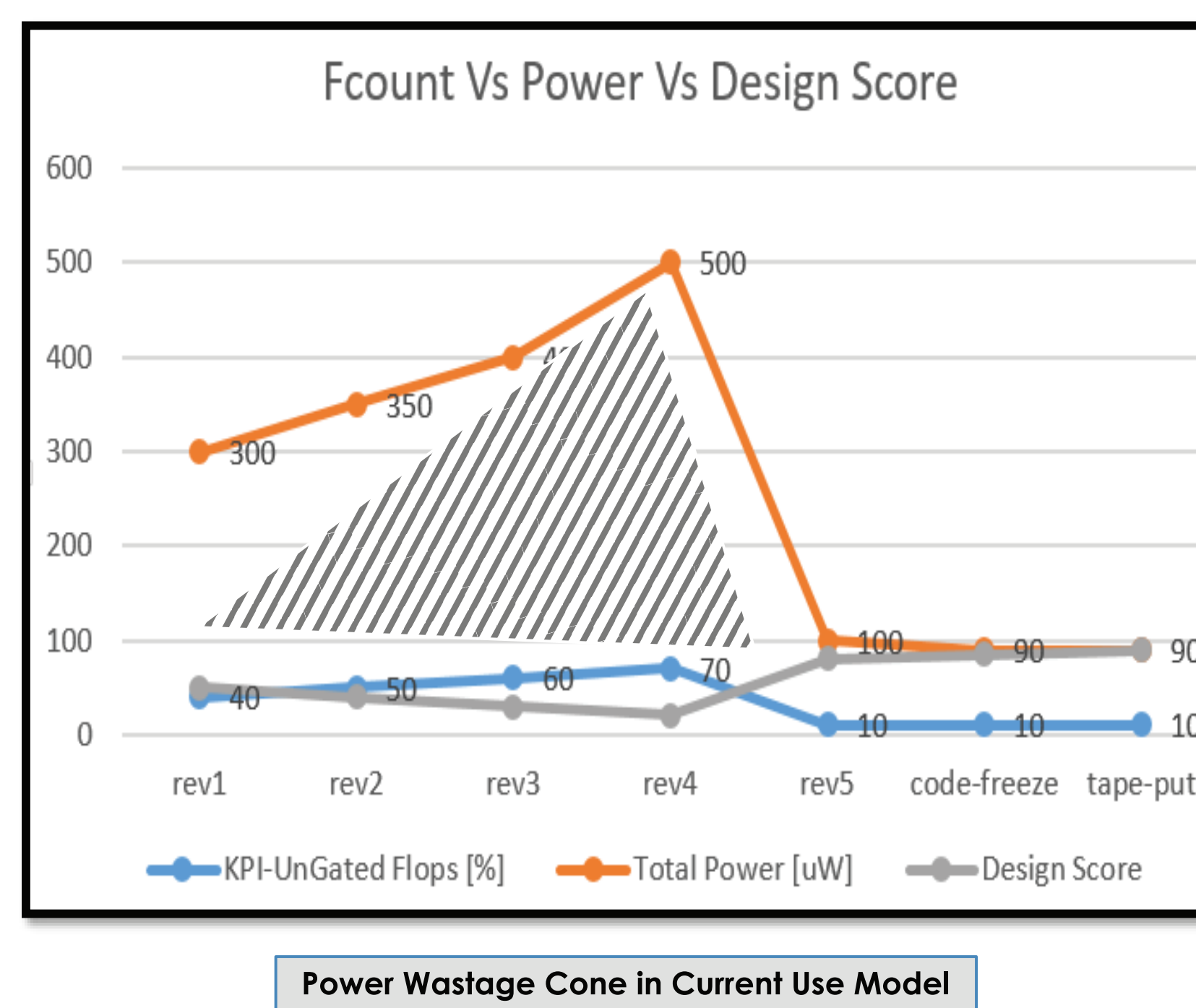
- IMetric driven approach help the designer/ management track the power scenario of the chip in much faster and easier way.
- Help different design companies define their own recipe of metric which is unknown to vendor, helps maintain confidentiality.
- Designer no more bound to standard tool output and free to define his/her own objectives which are clean and quick.
- Help in identifying the behavior of various key metrics for each revision and different usecases.
- User can define graded scores against various values of each metric thereby qualifying the block over a defined scale.
- Qualify the block for power — IP Power Qualification
- Help in quickly knowing the impact of fixes on redundancies in the design.
- Help in tracking various key metrics in terms of scores and absolute values.



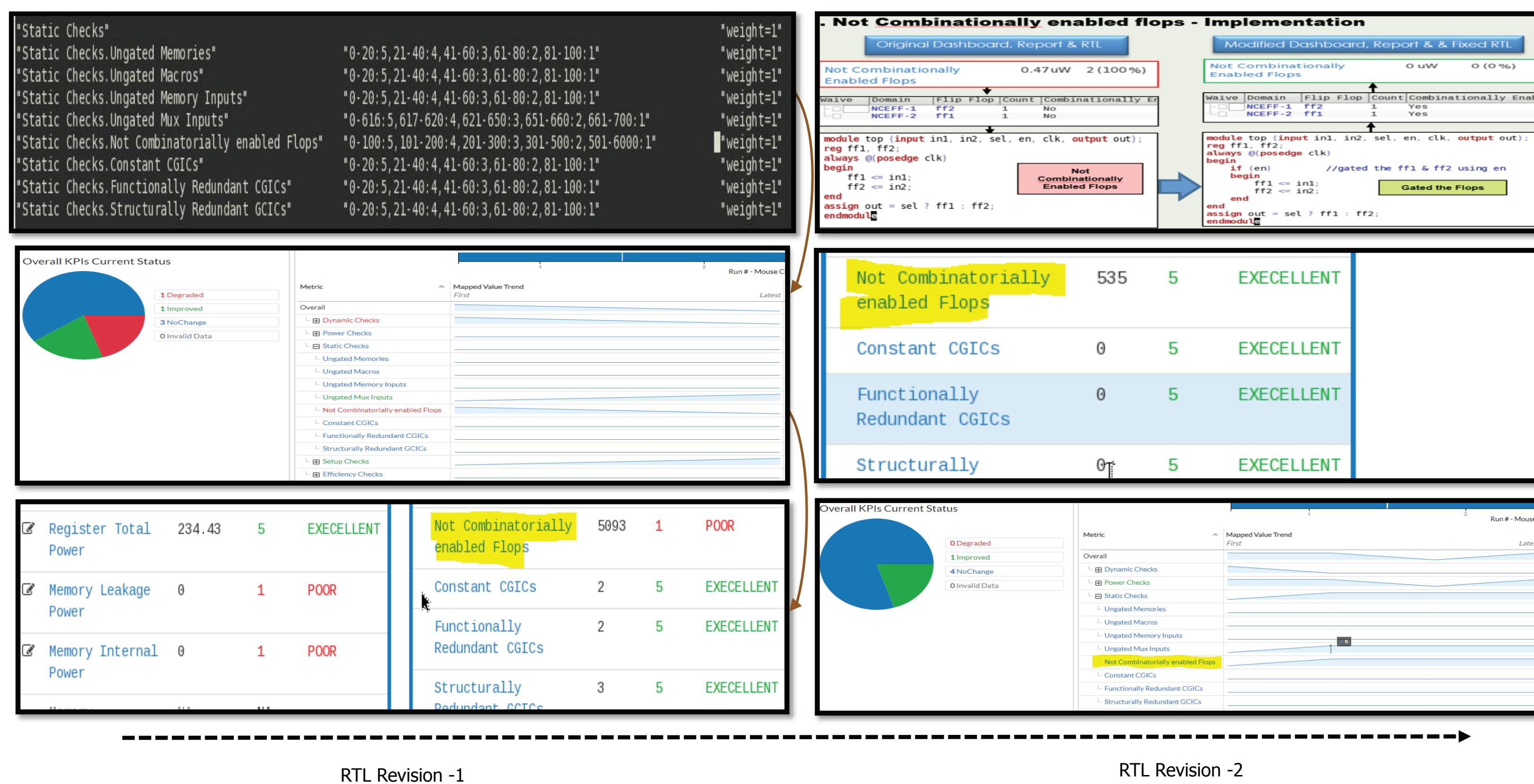
## Power Wastage Cone Current Model Vs Proposed

### Fixing Power Early on:

- Engaging early help fix more issues, saves more power
- Not leaving to last minute, time crunch might lead to sub-optimal fixes
- Power saving potential more at early RTL stage than on mature RTL stage



## MDPR Flow [Define, Identify, Fix and Track]



## Evidence & Summary

Design	Flop Count	Engaging Early, Fixing Upfront—No Last Minute Rush						
		Traditional Flow				Developed Flow		
		Power Saving Potential	Power Fixed	Power Wastage Left Unfixed	RTL Stage Reached [out of 10]	Power Fixed	Power Wastage Left Unfixed	RTL Stage Reached [out of 10]
Design 1	250K	50 uW	20 uW	30 uW	Sign-off	50 uW	0 uW	Revision 4
Design 2	300K	60 uW	15 uW	45 uW	Sign-off	55 uW	5 uW	Revision 5
Design 3	150K	40 uW	30 uW	10 uW	Sign-off	40 uW	0 uW	Revision 3

- Metric driven power regression flow provides automated means to define the standard/ proprietary power objectives [KPIs] for the block, report the failures, interactively help user fix them and provide sophisticated plots to monitor the power trends with each revision of RTL.
- In traditional methodology, vendor provided standard output is one-size-fits-all format. Therefore, metrics mechanism provides flexibility to define proprietary metrics and track them [unknown to vendor, third party].
- All this work in traditional methodology would require huge effort and time in fetching meaningful data from various reports, logs and commands. While the proposed solution fetches the user predefined data natively in much faster way- saving time and effort.
- Easily qualify the block/IP/chip for power and take necessary actions in terms of power reductions/architectural changes.
- Management has greater insight on power scenarios of the block/chip which otherwise required complete dependency on the tool user.